

### FEATURES

- 1.8 V to 5.5 V Single Supply
- 4  $\Omega$  (Max) On Resistance
- 0.75  $\Omega$  (Typ) On Resistance Flatness
- Automotive Temperature Range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- $-3$  dB Bandwidth  $> 200$  MHz
- Rail-to-Rail Operation
- 6-Lead SOT-23 Package and 8-Lead  $\mu\text{SOIC}$  Package
- Fast Switching Times:
  - $t_{\text{ON}} = 12$  ns
  - $t_{\text{OFF}} = 6$  ns
- Typical Power Consumption ( $< 0.01$   $\mu\text{W}$ )
- TTL/CMOS Compatible

### APPLICATIONS

- Battery-Powered Systems
- Communication Systems
- Sample-and-Hold Systems
- Audio Signal Routing
- Video Switching
- Mechanical Reed Relay Replacement

### GENERAL DESCRIPTION

The ADG719 is a monolithic CMOS SPDT switch. This switch is designed on a submicron process that provides low power dissipation yet gives high switching speed, low on resistance, and low leakage currents.

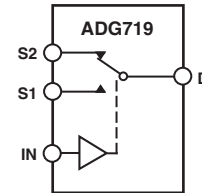
The ADG719 can operate from a single-supply range of 1.8 V to 5.5 V, making it ideal for use in battery-powered instruments and with the new generation of DACs and ADCs from Analog Devices.

Each switch of the ADG719 conducts equally well in both directions when on. The ADG719 exhibits break-before-make switching action.

Because of the advanced submicron process,  $-3$  dB bandwidths of greater than 200 MHz can be achieved.

The ADG719 is available in a 6-lead SOT-23 package and an 8-lead  $\mu\text{SOIC}$  package.

### FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC "1" INPUT

### PRODUCT HIGHLIGHTS

1. 1.8 V to 5.5 V Single-Supply Operation. The ADG719 offers high performance, including low on resistance and fast switching times, and is fully specified and guaranteed with 3 V and 5 V supply rails.
2. Very Low  $R_{\text{ON}}$  (4  $\Omega$  Max at 5 V and 10  $\Omega$  Max at 3 V). At 1.8 V operation,  $R_{\text{ON}}$  is typically 40  $\Omega$  over the temperature range.
3. Automotive Temperature Range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
4. On Resistance Flatness ( $R_{\text{FLAT(ON)}}$ ) (0.75  $\Omega$  typ).
5.  $-3$  dB Bandwidth  $> 200$  MHz.
6. Low Power Dissipation. CMOS construction ensures low power dissipation.
7. Fast  $t_{\text{ON}}/t_{\text{OFF}}$ .
8. Tiny 6-lead SOT-23 and 8-lead  $\mu\text{SOIC}$  packages.

### REV. B

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

# ADG719—SPECIFICATIONS<sup>1</sup> ( $V_{DD} = 5\text{ V} \pm 10\%$ , $GND = 0\text{ V}$ .)

Parameter	B Version			Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C	-40°C to +125°C		
<b>ANALOG SWITCH</b>					
Analogue Signal Range			0 V to $V_{DD}$	V	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_S = -10\text{ mA}$ ; Test Circuit 1
On Resistance ( $R_{ON}$ )	2.5			$\Omega$ typ	
	4	5	7	$\Omega$ max	
On Resistance Match Between Channels ( $\Delta R_{ON}$ )		0.1		$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_S = -10\text{ mA}$
		0.4	0.4	$\Omega$ max	
On Resistance Flatness ( $R_{FLAT(ON)}$ )	0.75	1.2	1.5	$\Omega$ typ	$V_S = 0\text{ V}$ to $V_{DD}$ , $I_S = -10\text{ mA}$
				$\Omega$ max	
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage $I_S$ (Off)	$\pm 0.01$			nA typ	$V_{DD} = 5.5\text{ V}$ $V_S = 4.5\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/4.5\text{ V}$ ; nA max Test Circuit 2 $V_S = V_D = 1\text{ V}$ or $V_S = V_D = 4.5\text{ V}$ ; nA max Test Circuit 3
Channel On Leakage $I_D$ , $I_S$ (On)	$\pm 0.25$	$\pm 0.35$	1	nA typ	
	$\pm 0.01$			nA typ	
	$\pm 0.25$	$\pm 0.35$	5	nA typ	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.4	V min	$V_{IN} = V_{INL}$ or $V_{INH}$
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current					
$I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	
			$\pm 0.1$	$\mu\text{A}$ max	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>					
$t_{ON}$	7			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$ ; Test Circuit 4
			12	ns max	
$t_{OFF}$	3			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$ ; Test Circuit 4
			6	ns max	
Break-Before-Make Time Delay, $t_D$	8			ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_{S1} = V_{S2} = 3\text{ V}$ ; Test Circuit 5
			1	ns min	
Off Isolation	-67			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 6
	-87			dB typ	
Channel-to-Channel Crosstalk	-62			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 7
	-82			dB typ	
Bandwidth -3 dB	200			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; Test Circuit 8
$C_S$ (Off)	7			pF typ	
$C_D$ , $C_S$ (On)	27			pF typ	
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = 5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V
			1.0	$\mu\text{A}$ max	

## NOTES

<sup>1</sup>Temperature range is as follows: B Version: -40°C to +125°C.

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

**SPECIFICATIONS<sup>1</sup>** ( $V_{DD} = 3\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ .)

Parameter	B Version			Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C	-40°C to +125°C		
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	6	7		$\Omega$ typ $\Omega$ max	$V_S = 0\text{ V to }V_{DD}$ , $I_S = -10\text{ mA}$ ; Test Circuit 1
On Resistance Match Between Channels ( $\Delta R_{ON}$ )		0.1	12	$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_S = -10\text{ mA}$
On Resistance Flatness ( $R_{FLAT(ON)}$ )		0.4	0.4	$\Omega$ max	
		2.5		$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_S = -10\text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source Off Leakage $I_S$ (Off)	$\pm 0.01$ $\pm 0.25$	$\pm 0.35$	1	nA typ nA max	$V_{DD} = 3.3\text{ V}$ $V_S = 3\text{ V}/1\text{ V}$ , $V_D = 1\text{ V}/3\text{ V}$ ; Test Circuit 2
Channel On Leakage $I_D$ , $I_S$ (On)	$\pm 0.01$ $\pm 0.25$	$\pm 0.35$	5	nA typ nA max	$V_S = V_D = 1\text{ V}$ or $V_S = V_D = 3\text{ V}$ ; Test Circuit 3
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005		$\pm 0.1$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>					
$t_{ON}$	10		15	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 2\text{ V}$ ; Test Circuit 4
$t_{OFF}$	4		8	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 2\text{ V}$ ; Test Circuit 4
Break-Before-Make Time Delay, $t_D$	8		1	ns typ ns min	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 2\text{ V}$ ; Test Circuit 5
Off Isolation	-67 -87			dB typ dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 6
Channel-to-Channel Crosstalk	-62 -82			dB typ dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 7
Bandwidth -3 dB	200			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; Test Circuit 8
$C_S$ (Off)	7			pF typ	
$C_D$ , $C_S$ (On)	27			pF typ	
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001		1.0	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{DD} = 3.3\text{ V}$ Digital Inputs = 0 V or 3.3 V

## NOTES

<sup>1</sup>Temperature range is as follows: B Version: -40°C to +125°C.<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# ADG719

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = 25°C, unless otherwise noted.)

V <sub>DD</sub> to GND	−0.3 V to +7 V
Analog, Digital Inputs <sup>2</sup>	−0.3 V to V <sub>DD</sub> + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D	100 mA (Pulsed at 1 ms, 10% Duty Cycle Max)
Continuous Current, S or D	30 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
μSOIC Package, Power Dissipation	315 mW
θ <sub>JA</sub> Thermal Impedance	206°C/W
θ <sub>JC</sub> Thermal Impedance	44°C/W
SOT-23 Package, Power Dissipation	282 mW
θ <sub>JA</sub> Thermal Impedance	229.6°C/W
θ <sub>JC</sub> Thermal Impedance	91.99°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD	1 kV

### NOTES

<sup>1</sup> Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

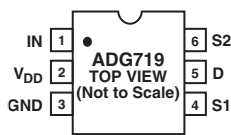
<sup>2</sup> Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

**Table I. Truth Table**

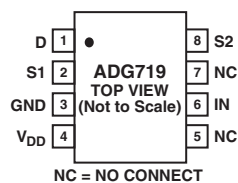
ADG719 IN	Switch S1	Switch S2
0	ON	OFF
1	OFF	ON

## PIN CONFIGURATIONS

**6-Lead SOT-23  
(RT-6)**



**8-Lead μSOIC  
(RM-8)**



## ORDERING GUIDE

Model	Temperature Range	Brand*	Package Description	Package Option
ADG719BRM	−40°C to +125°C	S5B	μSOIC (MicroSmall Outline IC) [MSOP]	RM-8
ADG719BRT	−40°C to +125°C	S5B	SOT-23 (Plastic Surface Mount)	RT-6

\*Branding on these packages is limited to three characters due to space constraints.

## CAUTION

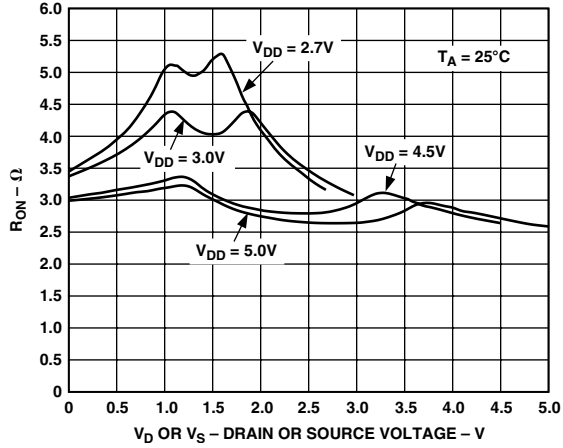
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG719 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## TERMINOLOGY

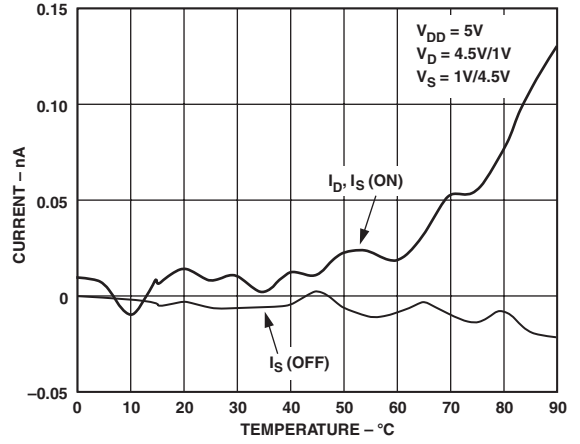
V <sub>DD</sub>	Most Positive Power Supply Potential
GND	Ground (0 V) Reference
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input
R <sub>ON</sub>	Ohmic Resistance between D and S
ΔR <sub>ON</sub>	On Resistance Match between Any Two Channels i.e., R <sub>ON max</sub> − R <sub>ON min</sub>
R <sub>FLAT(ON)</sub>	Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.
I <sub>S</sub> (Off)	Source Leakage Current with the Switch Off
I <sub>D</sub> , I <sub>S</sub> (On)	Channel Leakage Current with the Switch On
V <sub>D</sub> (V <sub>S</sub> )	Analog Voltage on Terminals D and S
C <sub>S</sub> (Off)	Off Switch Source Capacitance
C <sub>D</sub> , C <sub>S</sub> (On)	On Switch Capacitance
t <sub>ON</sub>	Delay between Applying the Digital Control Input and the Output Switching On
t <sub>OFF</sub>	Delay between Applying the Digital Control Input and the Output Switching Off
t <sub>D</sub>	Off Time or On Time Measured between the 90% Points of Both Switches, when Switching From One Address State to Another
Crosstalk	A Measure of Unwanted Signal That Is Coupled through from One Channel to Another as a Result of Parasitic Capacitance
Off Isolation	A Measure of Unwanted Signal Coupling through an Off Switch
Bandwidth	The Frequency at Which the Output is Attenuated by −3 dBs
On Response	The Frequency Response of the On Switch
Insertion Loss	Loss due to On Resistance of Switch



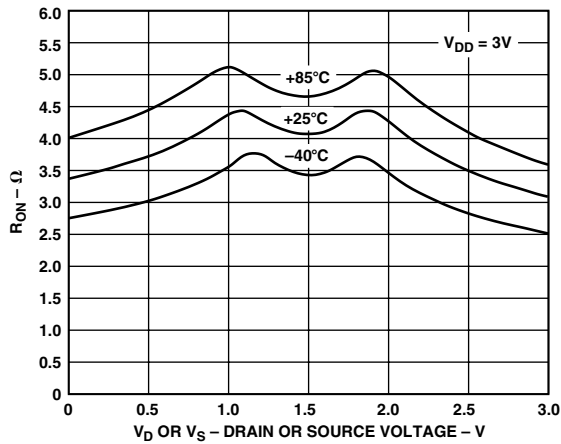
# Typical Performance Characteristics—ADG719



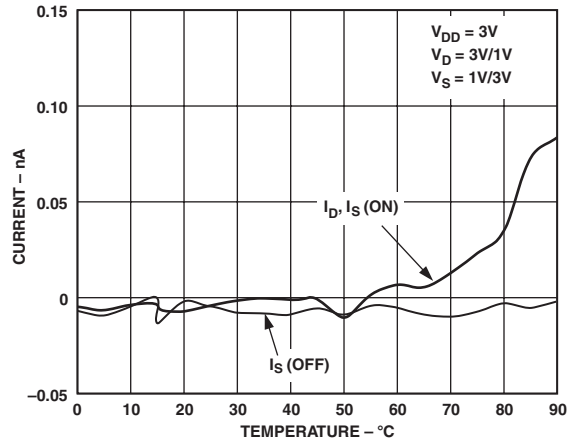
TPC 1. On Resistance vs.  $V_D$  ( $V_S$ ), Single Supplies



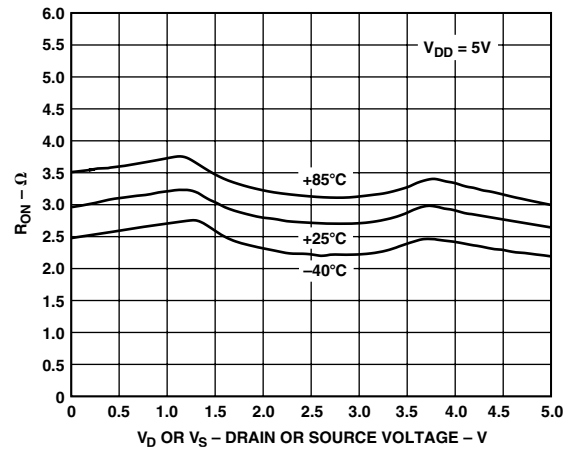
TPC 4. Leakage Currents vs. Temperature



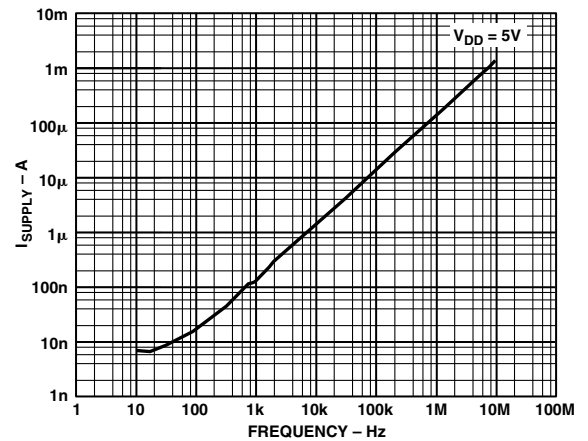
TPC 2. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures,  $V_{DD} = 3V$



TPC 5. Leakage Currents vs. Temperature

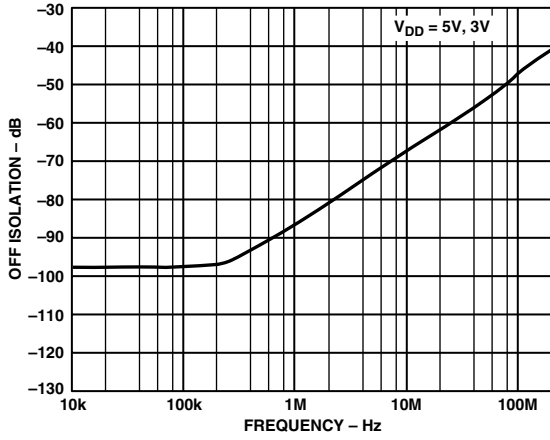


TPC 3. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures,  $V_{DD} = 5V$

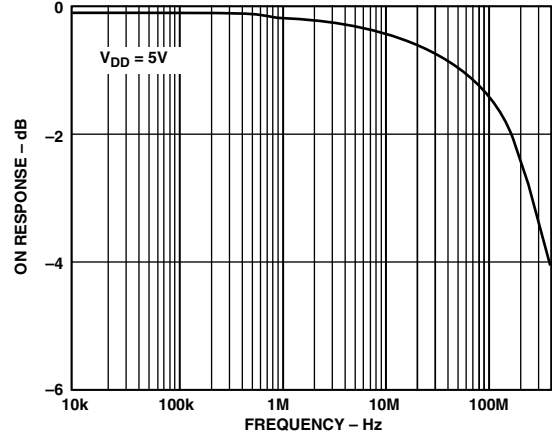


TPC 6. Supply Current vs. Input Switching Frequency

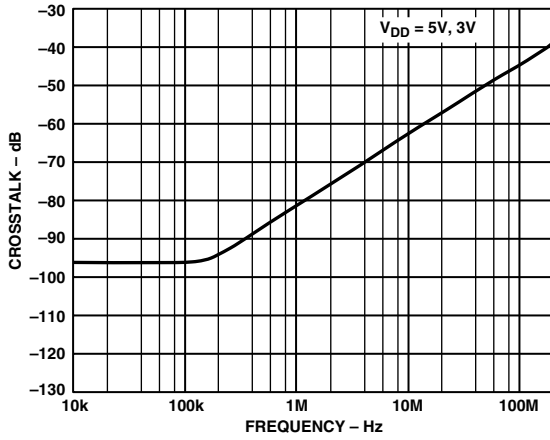
# ADG719



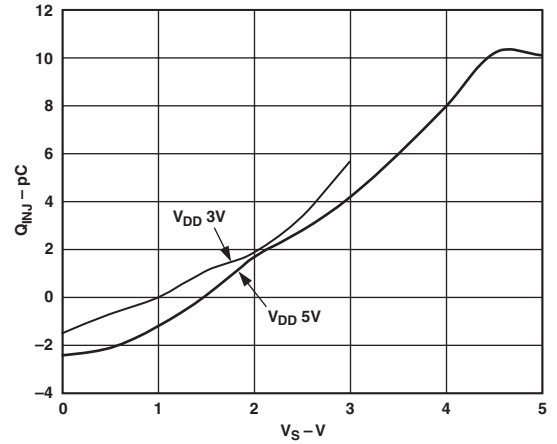
TPC 7. Off Isolation vs. Frequency



TPC 9. On Response vs. Frequency

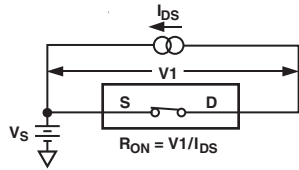


TPC 8. Crosstalk vs. Frequency

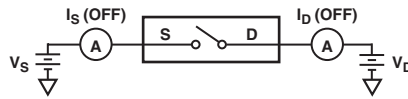


TPC 10. Charge Injection vs. Source Voltage

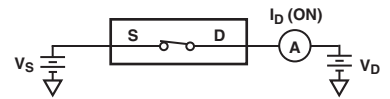
# Test Circuits



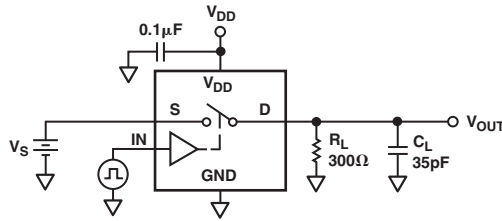
Test Circuit 1. On Resistance



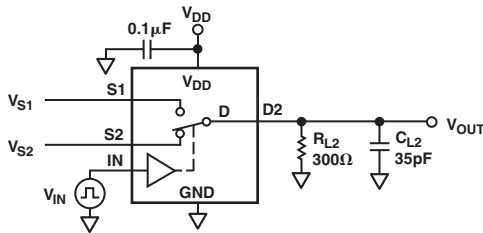
Test Circuit 2. Off Leakage



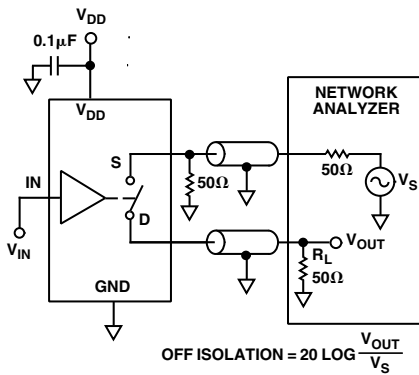
Test Circuit 3. On Leakage



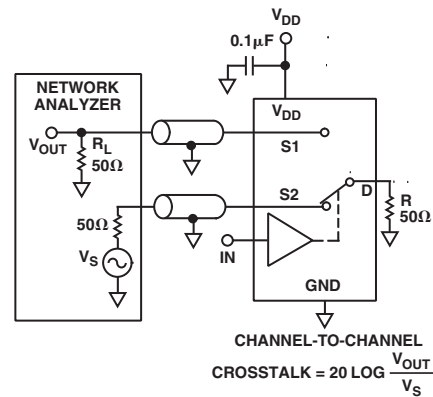
Test Circuit 4. Switching Times



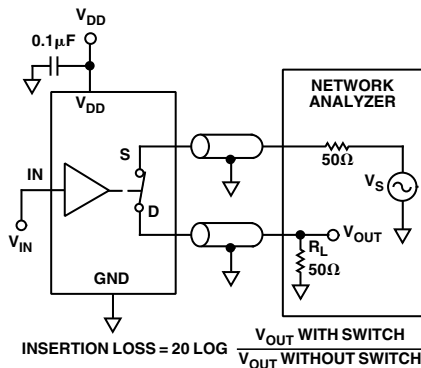
Test Circuit 5. Break-Before-Make Time Delay,  $t_D$



Test Circuit 6. Off Isolation



Test Circuit 7. Channel-to-Channel Crosstalk



Test Circuit 8. Bandwidth

# ADG719

## APPLICATIONS INFORMATION

The ADG719 belongs to Analog Devices' new family of CMOS switches. This series of general-purpose switches has improved switching times, lower on resistance, higher bandwidths, low power consumption, and low leakage currents.

### ADG719 Supply Voltages

Functionality of the ADG719 extends from 1.8 V to 5.5 V single supply, which makes it ideal for battery-powered instruments where power efficiency and performance are important design parameters.

It is important to note that the supply voltage effects the input signal range, the on resistance, and the switching times of the part. By taking a look at the Typical Performance Characteristics and the Specifications, the effects of the power supplies can be clearly seen.

For  $V_{DD} = 1.8$  V operation,  $R_{ON}$  is typically 40  $\Omega$  over the temperature range.

### On Response vs. Frequency

Figure 1 illustrates the parasitic components that affect the ac performance of CMOS switches (the switch is shown surrounded by a box). Additional external capacitances will further degrade some performance. These capacitances affect feedthrough, crosstalk, and system bandwidth.

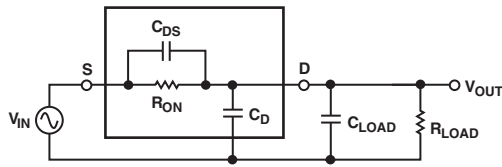


Figure 1. Switch Represented by Equivalent Parasitic Components

The transfer function that describes the equivalent diagram of the switch (Figure 1) is of the form  $A(s)$  shown below:

$$A(s) = R_T \left[ \frac{s(R_{ON} C_{DS}) + 1}{s(R_T R_{ON} C_T) + 1} \right]$$

where:

$$R_T = R_{LOAD} / (R_{LOAD} + R_{ON})$$

$$C_T = C_{LOAD} + C_D + C_{DS}$$

The signal transfer characteristic is dependent on the switch channel capacitance,  $C_{DS}$ . This capacitance creates a frequency zero in the numerator of the transfer function  $A(s)$ . Because the switch on resistance is small, this zero usually occurs at high frequencies. The bandwidth is a function of the switch output capacitance combined with  $C_{DS}$  and the load capacitance. The frequency pole corresponding to these capacitances appears in the denominator of  $A(s)$ .

The dominant effect of the output capacitance,  $C_D$ , causes the pole breakpoint frequency to occur first. Therefore, in order to maximize bandwidth, a switch must have a low input and output capacitance and low on resistance. The On Response vs. Frequency plot for the ADG719 can be seen in TPC 9.

### Off Isolation

Off isolation is a measure of the input signal coupled through an off switch to the switch output. The capacitance,  $C_{DS}$ , couples the input signal to the output load when the switch is off, as shown in Figure 2.

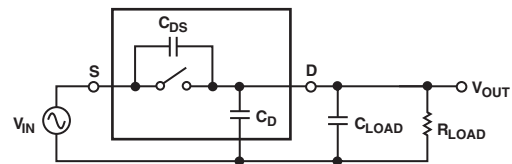


Figure 2. Off Isolation Is Affected by External Load Resistance and Capacitance

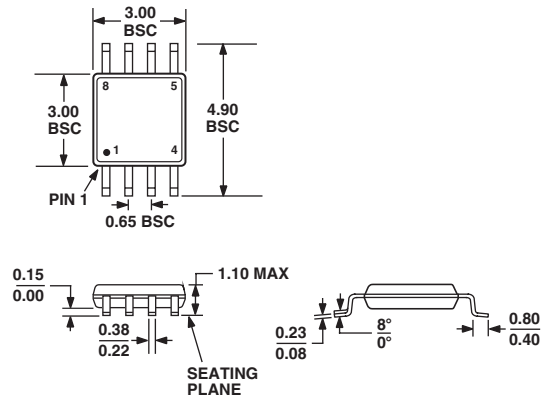
The larger the value of  $C_{DS}$ , the larger the values of feedthrough that will be produced. TPC 7 illustrates the drop in off isolation as a function of frequency. From dc to roughly 200 kHz, the switch shows better than -95 dB isolation. Up to frequencies of 10 MHz, the off isolation remains better than -67 dB. As the frequency increases, more and more of the input signal is coupled through to the output. Off isolation can be maximized by choosing a switch with the smallest  $C_{DS}$  possible. The values of load resistance and capacitance also affect off isolation, since they contribute to the coefficients of the poles and zeros in the transfer function of the switch when open.

$$A(s) = \left[ \frac{s(R_{LOAD} C_{DS})}{s(R_{LOAD})(C_{LOAD} + C_D + C_{DS}) + 1} \right]$$



**OUTLINE DIMENSIONS**  
**8-Lead Small Outline Package [MSOP]**  
**(RM-8)**

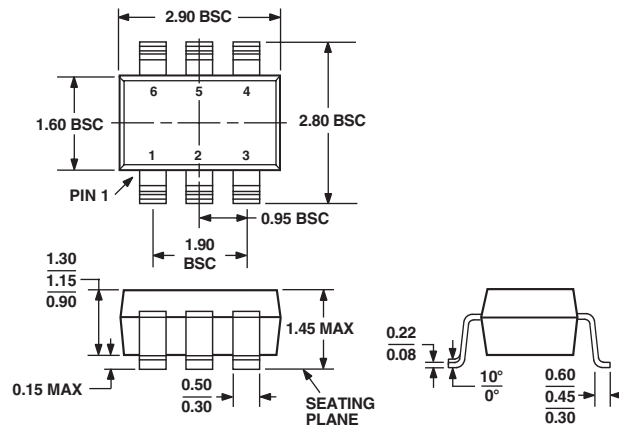
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187AA

**6-Lead Plastic Surface Mount Package [SOT-23]**  
**(RT-6)**

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178AB

# ADG719

## Revision History

<b>Location</b>	<b>Page</b>
<b>7/02 Data Sheet changed from REV. A to REV. B.</b>	
Changes to Product Name .....	1
Changes to FEATURES .....	1
Additions to PRODUCT HIGHLIGHTS .....	1
Changes to SPECIFICATIONS .....	2
Edits to ABSOLUTE MAXIMUM RATINGS .....	4
Changes to TERMINOLOGY .....	4
Edits to ORDERING GUIDE .....	4
Added new TPCs 4 and 5 .....	5
Replaced TPC 10 .....	6
TEST CIRCUITs 6, 7, and 8 replaced .....	7
Updated RM-8 and RT-6 package outlines .....	9



