MY18E20 MY1820 MY18B20Z MY18B20L
±0.5℃、12bit ADC、Low power consumption、1-wire interface Digital Thermometer

1. Overview

MY18E20、MY1820、MY18B20Z and MY18B20L are digital high-precision temperature sensor with a typical temperature measurement accuracy of 0.5 ℃. The temperature sensing principle is based on the characteristic relationship between the semiconductor PN-junction temperature and voltage, through small signal amplification, analog to digital conversion and digital calibration, the 12-bit digital temperature data can be easily accessed. It has strength of high accuracy and consistency, long lifetime, low power consumption, programmable configuration flexibility. The thermometer integrates an EEPROM as a storage for ROM ID of the sensors, temperature alarm threshold, temperature calibration correction values and user-defined information such as sensor node information. Each sensor IC has a unique 64-bit serial number as ROM ID, and is fully calibrated before ship out. The IC has one-wire interface for the host processor to access.

2. Features

- Highest accuracy:
  ±0.5℃ from -10°C to +85°C
- Measures Temperatures from -55 ℃ to +125°C (-67°F to +257°F)
- Typical standby power consumption is 0.2 μA@5V, average temperature measurement current is 5μA @1Hz
- Wide supply voltage range 1.8V-5.5V
- The standard to the series has a default 12-bit ADC output with resolution of 0.0625°C, and can also be programmed to 14-bit ADC output, with a resolution of 0.0125°C
- Configurable conversion time: 500ms/15ms
- 80-bit Non-Volatile Memory (NVM) space for user data storage
- Every thermometer has a unique ROM ID for easy network addressing
- User configurable alarm threshold
- One-wire interface

3. Applications

- Environmental temperature monitoring
- Smart hardware
- Agricultural temperature monitoring
- Instruments and Apparatuses
- Smart home
- Multipoint series temperature measurement

Part Number	Package	Temperature Conversion Time
MY18E20	TO-92	500ms
MY18E20-15	TO-92	15ms
MY1820	TO92S	500ms
MY1820-15	TO92S	15ms
MY18B20Z	SOP8	500ms
MY18B20Z-15	SOP8	15ms
MY18B20L	TO-92L	500ms
MY18B20L-15	TO-92L	15ms

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4. Package pin description

4.1 MY18E20/MY18E20-15（TO-92）

Front View

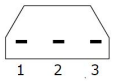
Bottom view

Physical Photo

No.	Pin Name	I/O	Description
1	GND	—	Ground
2	DQ	IO	One-wire data line
3	VDD	—	Power

4.2 MY1820/MY1820-15（TO92S）

Front View



Bottom view

Physical Photo

No.	Pin Name	I/O	Description
1	GND	—	Ground
2	DQ	IO	One-wire data line
3	VDD	—	Power

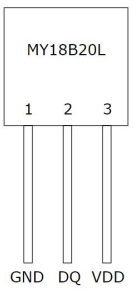
4.3 MY18B20Z/MY18B20Z-15（SOP8）

Vertical View

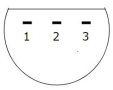
Physical Photo

No.	Pin Name	I/O	Description
1	N.C.	—	No Connection
2	N.C.	—	No Connection
3	VDD	—	Power
4	DQ	IO	One-wire data line
5	GND	—	Ground
6	N.C.	—	No Connection
7	N.C.	—	No Connection
8	N.C.	—	No Connection

4.4 MY18B20L/MY18B20L-15（TO-92L）



Front View

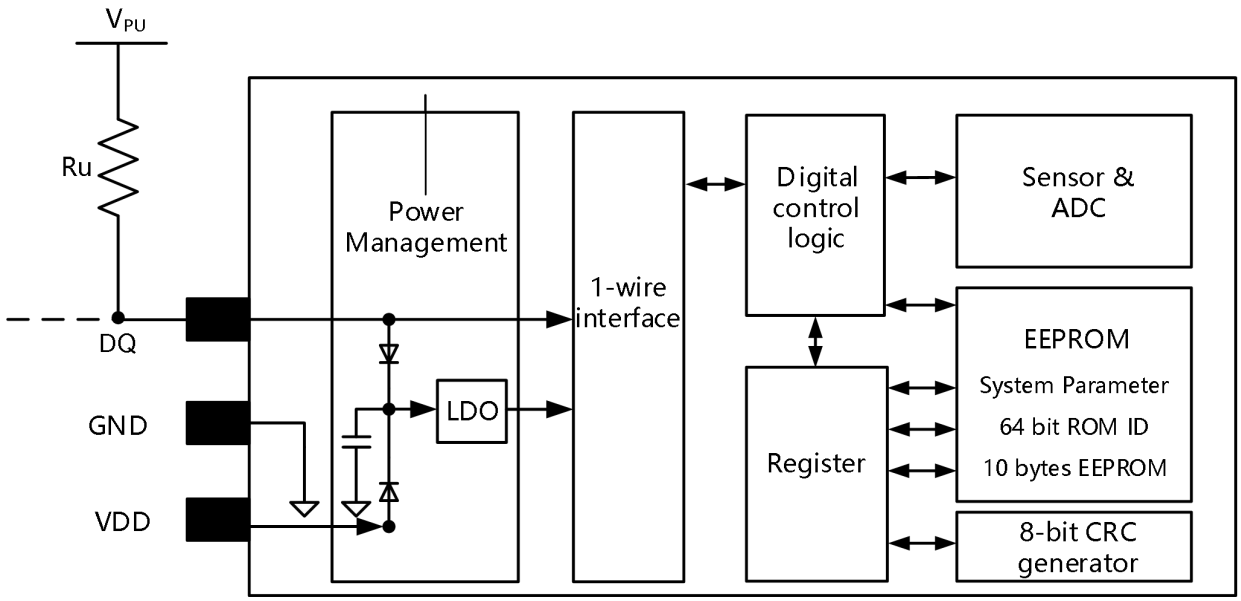


Bottom view

Physical Photo

No.	Pin Name	I/O	Description
1	GND	—	Ground
2	DQ	IO	One-wire data line
3	VDD	—	Power

5. System Diagram

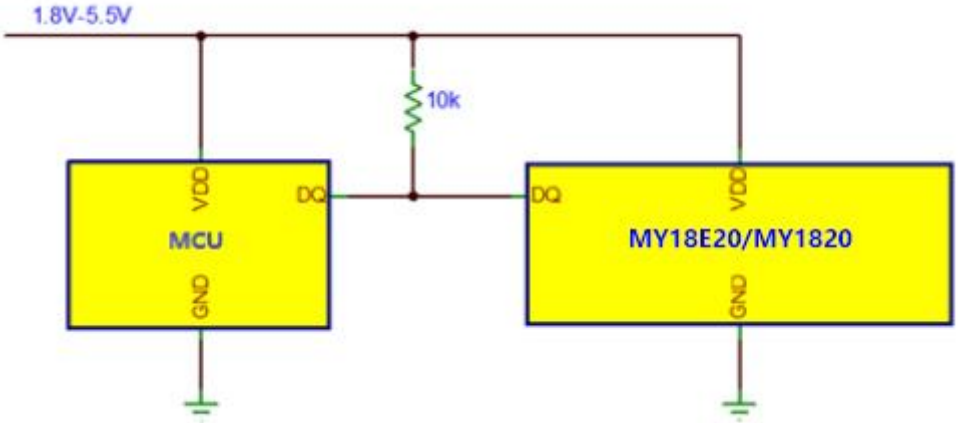


Note: The internal system composition of the sensor takes MY18E20 as an example, and other part number are the same.

The figure above shows the schematic diagram of the temperature sensor. The 64 bit ROM stores the unique ID serial number of the device. The register contains two bytes of temperature register, which stores the digital output from the sensor. In addition, the scratchpad provides access to the 1-byte upper and lower alarm trigger registers (TH and TL) and the 1-byte configuration register. The configuration register allows the user to set the resolution of the temperature-to-digital conversion to 9, 10, 11, or 12 bits. 14 bit resolution needs to be customized. In addition, 10 bytes of data space is provided for users to use. Data can be stored in nonvolatile memory, and data will not be lost when the chip is powered down.

The MY18E20 uses Maxim’ s exclusive 1-Wire bus protocol that implements bus communication using one control signal. The control line requires a weak pullup resistor since all devices are linked to the bus via a 3-state or open-drain port (the DQ pin in the case of the MY18E20). In this bus system, the microprocessor (the master device) identifies and addresses devices on the bus using each device’ s unique 64-bit code. Because each device has a unique code, the number of devices that can be addressed on one bus is virtually unlimited. The 1-Wire bus protocol, including detailed explanations of the commands and “time slots,” is covered in the 1-Wire Bus System section.

6. Typical Application



Notes：1 Under long cable or multi-point driving conditions, please ensure that the power supply voltage is more than 3.3V as far as possible.

2 Under the condition of long cable or multi-point drive, 1K resistance is preferred for pull-up resistance.

3 Under the condition of 5V voltage and 1K pull-up resistance,100 PCS MY18E20/ MY1820/MY18B20Z/ MY18B20L can be connected in a single bus, and the maximum length of the cable can be up to 500m.

7. Operation

7.1 Operation - Measuring Temperature

The core functionality of the MY18E20/MY1820/MY1820Z/MY18B20L is its direct-to-digital temperature sensor (The following contents take MY18E20 as an example, and other part numbers are the same) . The resolution of the temperature sensor is user-configurable to 9, 10, 11, or 12 bits, corresponding to increments of 0.5°C, 0.25°C, 0.125°C, and 0.0625°C, respectively. The default resolution at power-up is 12-bit. The MY18E20 powers up in a low-power idle state. To initiate a temperature measurement and A-to-D conversion, the master must issue a Convert T [44h] command. Following the conversion, the resulting thermal data is stored in the 2-byte temperature register in the scratchpad memory and the MY18E20 returns to its idle state. If the MY18E20 is powered by an external supply, the master can issue "read time slots" (see the 1-Wire Bus System section) after the Convert T command and the MY18E20 will respond by transmitting 0 while the temperature conversion is in progress and 1 when the con- version is done.

The MY18E20 output temperature data is calibrated in degrees Celsius; for Fahrenheit applications, a lookup table or conversion routine must be used. The temperature data is stored as a 16-bit sign-extended two' s complement number in the temperature register (see Figure 7.1-1， Figure 7.1-2). The sign bits (S) indicate if the temperature is positive or negative: for positive numbers S = 0 and for negative numbers S = 1. If the MY18E20 is configured for 12-bit resolution, all bits in the temperature register will contain valid data. For 11-bit resolution, bit 0 is undefined. For 10-bit resolution, bits 1 and 0 are undefined, and for 9-bit resolution bits 2, 1, and 0 are undefined. Table

7.1-1 and Table 7.1-2 give examples of digital output data and the corresponding temperature reading for 12-bit and 14-bit resolution conversions respectively.

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
LS BYTE	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
MS BYTE	S	S	S	S	S	2^6	2^5	2^4

Figure7.1-1 Temperature Register Format(9~12-bit)

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
LS BYTE	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
MS BYTE	2^{-5}	2^{-6}	S	S	S	2^6	2^5	2^4

Figure7.1-2 Temperature Register Format（14-bit）

Table7.1-1 Temperature/Data Relationship（12bit）

TEMPERATURE (°C)	DIGITAL OUTPUT(BINARY)	DIGITAL OUTPUT(HEX)
+125	0000 0111 1101 0000	07D0h
+85	0000 0101 0101 0000	0550h
+25.0625	0000 0001 1001 0001	0191h
+10.125	0000 0000 1010 0010	00A2h
+0.5	0000 0000 0000 1000	0008h
0	0000 0000 0000 0000	0000h
-0.5	1111 1111 1111 1000	FFF8h
-10.125	1111 1111 0101 1110	FF5Eh
-25.0625	1111 1110 0110 1111	FE6Fh
-55	1111 1100 1001 0000	FC90h

Table7.1-2 Temperature/Data Relationship（14bit）

TEMPERATURE (°C)	DIGITAL OUTPUT(BINARY)	DIGITAL OUTPUT(HEX)
+125	0000 0111 1101 0000	07D0h
+85	0000 0101 0101 0000	0550h
+45	0000 0010 1101 0000	02D0h
+42.5	0000 0010 1010 1000	02A8h
+42.125	0000 0010 1010 0010	02A2h
+40.046875	1100 0010 1000 0000	C280h
+40.015625	0100 0010 1000 0000	4280h
+38.25	0000 0010 0110 0100	0264h

+38.0625	0000 0010 0110 0001	0261h
+36.125	0000 0010 0100 0010	0242h
+36.015625	0100 0010 0100 0000	4240h
+35.03125	1000 0010 0011 0000	8230h
0	0000 0000 0000 0000	0000h
-35.03125	1011 1101 1100 1111	BDCFh
-36.015625	1111 1101 1011 1111	FDBFh
-36.125	0011 1101 1011 1110	3DBEh
-38.0625	0011 1101 1001 1111	3D9Fh
-38.25	0011 1101 0101 1000	3D9Ch
-40.015625	1111 1101 0111 1111	FD7Fh
-40.046875	0111 1101 0111 1111	7D7Fh
-42.125	0011 1101 0101 1110	3D5Eh
-42.5	0011 1101 0101 1000	3D58h
-45	0011 1111 1101 0011	3FD3h
-55	0011 1111 0010 0100	3F24h

7.2 Alarm

After the MY18E20 performs a temperature conversion, the temperature value is compared to the user-defined two' s complement alarm trigger values stored in the1-byte T_H and T_L registers (see Figure 7.2). The sign bit (S) indicates if the value is positive or negative: for positive numbers S=0 and for negative numbers S=1. The T_H and T_L registers are nonvolatile (EEPROM) so they will retain data when the device is powered down. T_H and T_L can be accessed through bytes 2 and 3 of the scratchpad as explained in the Memory section.

Only bits 11 through 4 of the temperature register are used in the T_H and T_L comparison since T_H and T_L are 8-bit registers. If the measured temperature is lower than or equal to T_L or higher than or equal to T_H, an alarm condition exists and an alarm flag is set inside the MY18E20. This flag is updated after every temperature measurement; therefore, if the alarm condition goes away, the flag will be turned off after the next temperature conversion.

The master device can check the alarm flag status of all MY18E20s on the bus by issuing an Alarm Search [ECh] command. Any MY18E20s with a set alarm flag will respond to the command, so the master can determine exactly which MY18E20s have experienced an alarm condition. If an alarm condition exists and the TH or TL settings have changed, another temperature conversion should be done to validate the alarm condition.

	ADDR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
(TH)	2	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
		bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8
(TL)	3	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Figure7.2 T_H和 T_L Register Format

8. Power

The MY18E20 can be powered by an external supply on the VDD pin (see Figure 8).The advantage of this mode is that MOSFET pull-up is not required, and the single bus can perform other operations at will during the temperature conversion process.

The master can issue a Skip ROM [CCh] command followed by a Read Power Supply [B4h] command followed by a "read time slot" . During the read time slot, externally powered MY18E20 will let the bus remain high.

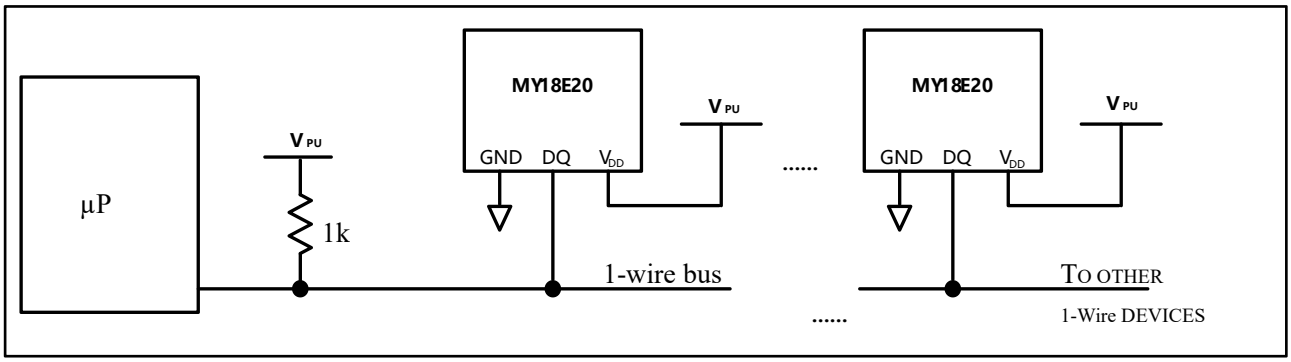


Figure 8 Powering the MY18E20

9. Memory

9.1 64-bit ROM code

Each MY18E20 contains a unique 64–bit code (see Figure 9.1) stored in ROM. The least significant 8 bits of the ROM code contain the MY18E20' s 1-Wire family code: 28h. The next 48 bits contain a unique serial number. The most significant 8 bits contain a cyclic redundancy check (CRC) byte that is calculated from the first 56 bits of the ROM code. A detailed explanation of the CRC bits is provided in the CRC Generation section. The 64-bit ROM code and associated ROM function control logic allow the MY18E20 to operate as a 1-Wire device using the protocol detailed in the 1-Wire Bus System section.

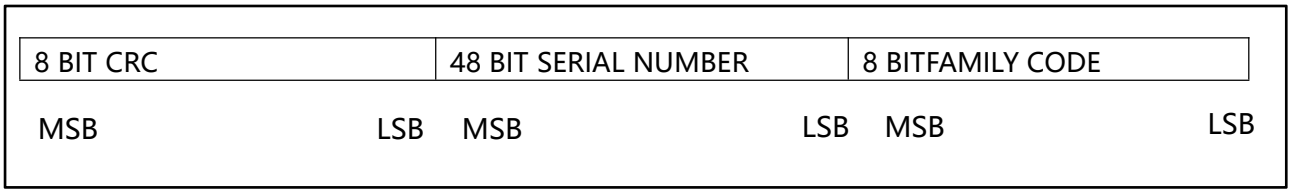


Figure 9.1 64-Bit ROM Code

9.2 Memory organization and access

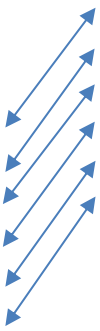
The MY18E20' s memory is organized as shown in Figure 9.2. The memory consists of an SRAM scratchpad with nonvolatile EEPROM storage for the high and low alarm trigger registers (TH and TL) and configuration register. Note that if the MY18E20 alarm function is not used, the TH and TL

registers can serve as general-purpose memory. All memory commands are described in detail in the MY18E20 Function Commands section. Byte 0 and byte 1 of the scratchpad contain the LSB and the MSB of the temperature register, respectively. These bytes are read-only. Bytes 2 and 3 provide access to TH and TL registers. Byte 4 contains the configuration register data, which is explained in detail in the Configuration Register section. Bytes 5, 6, and 7 are reserved for internal use by the device and cannot be overwritten. Byte 8 of the scratchpad is read-only and contains the CRC code for bytes 0 through 7 of the scratchpad. The MY18E20 generates this CRC using the method described in the CRC Generation section.

Data is written to bytes 2, 3, and 4 of the scratchpad using the Write Scratchpad [4Eh] command; the data must be transmitted to the MY18E20 starting with the least significant bit of byte 2. To verify data integrity, the scratchpad can be read (using the Read Scratchpad [BEh] command) after the data is written. When reading the scratchpad, data is transferred over the 1-Wire bus starting with the least significant bit of byte 0. To transfer the T_H, T_L and configuration data from the scratchpad to EEPROM, the master must issue the Copy Scratchpad [48h] command.

Data in the EEPROM registers is retained when the device is powered down; at power-up the EEPROM data is reloaded into the corresponding scratchpad locations. Data can also be reloaded from EEPROM to the scratch- pad at any time using the Recall E2 [B8h] command. The master can issue read time slots following the Recall E2 command and the MY18E20 will indicate the status of the recall by transmitting 0 while the recall is in progress and 1 when the recall is done.

BYTE	SCRATCHPAD	TYPE
0	TEMPERATURE LSB(50h)	READ
1	TEMPERATURE MSB (05h)	READ
2	TH Register	READ/WRITE
3	TLRegister	READ/WRITE
4	CONFIGURATION REGISTER	READ/WRITE
5	USER BYTE 3	READ/WRITE
6	USER BYTE 4	READ/WRITE
7	USER BYTE 5	READ/WRITE
8	CRC	READ



TH REGISTER OR USER BYTE 1
TL REGISTER OR USER BYTE 2T
CONFIGURATION REGISTER
USER BYTE 3
USER BYTE 4
USER BYTE 5
USER BYTE 6
...
USER BYTE 10

E^2PROM

Figure 9.2 MY18E20 Memory Map

9.3 Configuration Register

Byte 4 of the scratchpad memory contains the configuration register, which is organized as illustrated in Figure 9.3. The user can set the conversion resolution of the MY18E20 using the R0 and R1 bits in this register as shown in Table 9.3. The power-up default of these bits is R0 = 1 and R1 = 1 (12-bit resolution). Note that the conversion time can be programmed with each resolution option. Bit 7 and bits 0 to 4 in the configuration register are reserved for internal use by the device and cannot be overwritten.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	R1	R0	1	1	1	1	1

Figure 9.3 Configuration Register

Table9.3 Thermometer Resolution Configuration

R1	R0	RESOLUTION (BITS)	MAX CONVERSION TIME	
0	0	9-bit	15/100/500ms	tCONV
0	1	10-bit	15/100/500ms	tCONV
1	0	11-bit	15/100/500ms	tCONV
1	1	12-bit	15/100/500ms	tCONV
		14-bit	15/100/500ms	tCONV

9.4 CRC Generation

CRC bytes are provided as part of the MY18E20’ s 64-bit ROM code and in the 9th byte of the scratchpad memory. The ROM code CRC is calculated from the first 56 bits of the ROM code and is contained in the most significant byte of the ROM. The scratchpad CRC is calculated from the data stored in the scratchpad, and therefore it changes when the data in the scratchpad changes. The CRCs provide the bus master with a method of data validation when data is read from the MY18E20. To verify that data has been read correctly, the bus master must re-calculate the CRC from the received data and then compare this value to either the ROM code CRC (for ROM reads) or to the scratchpad CRC (for scratchpad reads). If the calculated CRC matches the read CRC, the data has been received error free. The comparison of CRC values and the decision to continue with an operation are determined entirely by the bus master. There is no circuitry inside the MY18E20 that prevents a command sequence from proceeding if the MY18E20 CRC (ROM or scratchpad) does not match the value generated by the bus master. The equivalent polynomial function of the CRC (ROM or scratchpad) is:

$$CRC = X^8 + X^5 + X^4 + 1$$

The bus master can recalculate the CRC and compare it to the CRC values from the MY18E20 using the polynomial generator shown in Figure 9.4. This circuit consists of a shift register and XOR gates, and the shift register bits are initialized to 0. Starting with the least significant bit of the ROM code or the least significant bit of byte 0 in the scratchpad, one bit at a time should shifted into the shift register. After shifting in the 56th bit from the ROM or the most significant bit of byte 7 from the scratchpad, the polynomial generator will contain the recalculated CRC. Next, the 8-bit ROM code or scratchpad CRC from the MY18E20 must be shifted into the circuit. At this point, if the re-calculated CRC was correct, the shift register will contain all 0s.

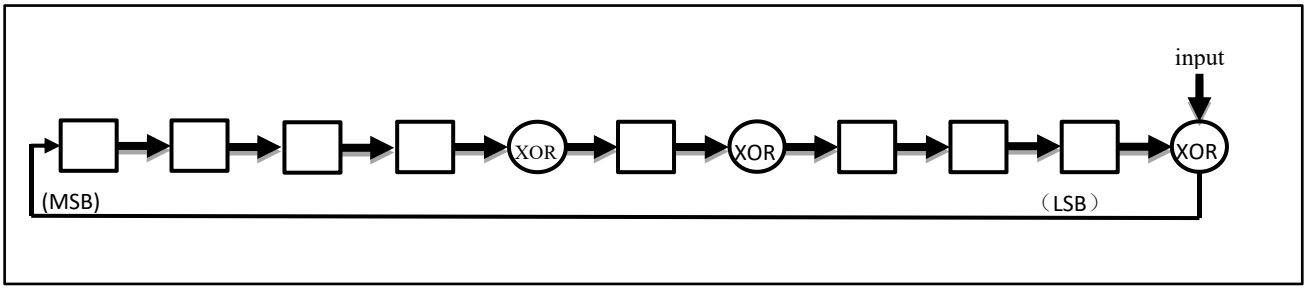


Figure 9.4 CRC Generator

10. 1-Wire Bus System

The 1-Wire bus system uses a single bus master to control one or more slave devices. The MY18E20 is always a slave. When there is only one slave on the bus, the system is referred to as a "single-drop" system; the system is "multi-drop" if there are multiple slaves on the bus. All data and commands are transmitted least significant bit first over the 1-Wire bus. The following discussion of the 1-Wire bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing).

10.1 Hardware Configuration

The 1-Wire bus has by definition only a single data line. Each device (master or slave) interfaces to the data line via an open-drain or 3-state port. This allows each device to "release" the data line when the device is not transmitting data so the bus is available for use by another device. The 1-Wire port of the MY18E20 (the DQ pin) is open drain with an internal circuit equivalent to that shown in Figure 10.1.

The 1-Wire bus requires an external pullup resistor of approximately 4.7kΩ; thus, the idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. Infinite recovery time can occur between bits so long as the 1-Wire bus is in the inactive (high) state during the recovery period. If the bus is held low for more than 480μs, all components on the bus will be reset.

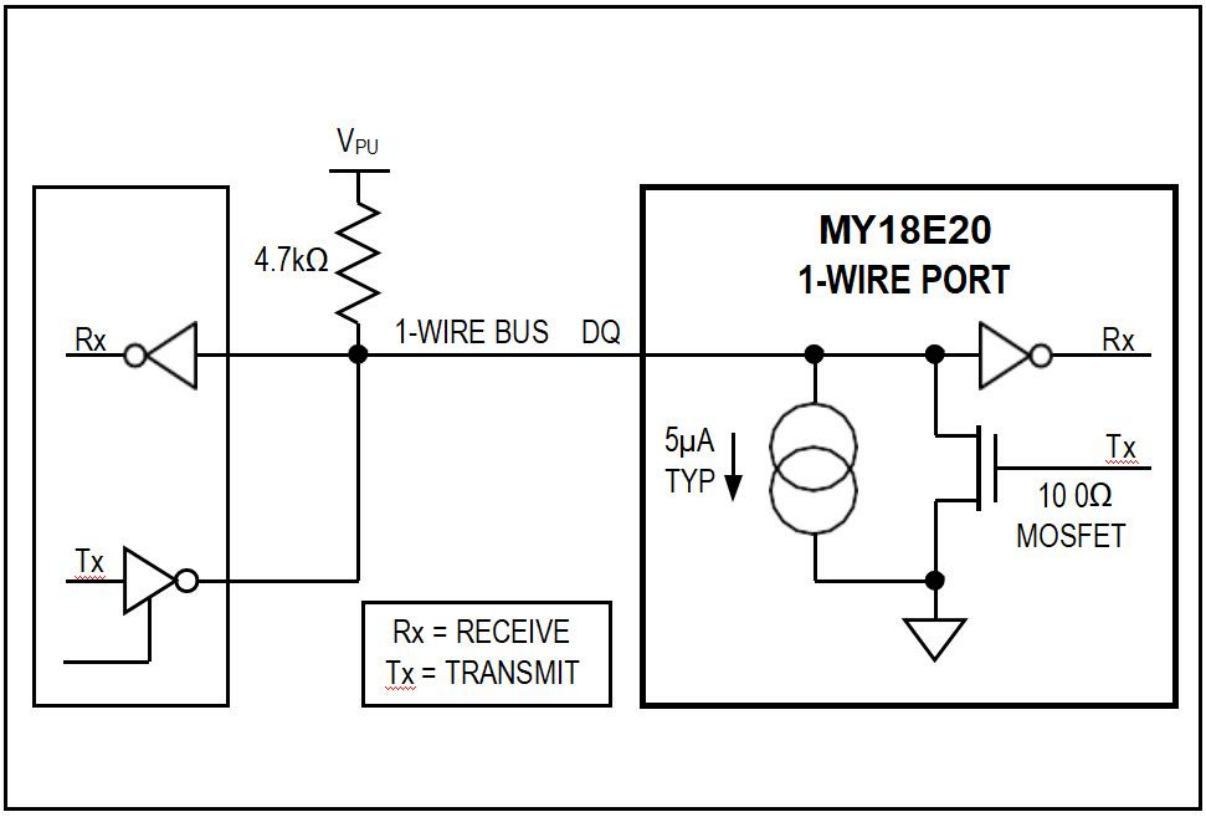


Figure 10.1 Hardware Configuration

10.2 Transaction Sequence

The transaction sequence for accessing the MY18E20 is as follows:
Step 1. Initialization
Step 2. ROM Command (followed by any required data exchange)
Step 3. MY18E20 Function Command (followed by any required data exchange)

It is very important to follow this sequence every time the MY18E20 is accessed, as the MY18E20 will not respond if any steps in the sequence are missing or out of order. Exceptions to this rule are the Search ROM [F0h] and Alarm Search [ECh] commands. After issuing either of these ROM commands, the master must return to Step 1 in the sequence.

10.3 Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that slave devices (such as the MY18E20) are on the bus and are ready to operate. Timing for the reset and presence pulses is detailed in the 1-Wire Signaling section.

10.4 ROM Commands

After the bus master has detected a presence pulse, it can issue a ROM command. These commands operate on the unique 64-bit ROM codes of each slave device and allow the master to single out a specific device if many are present on the 1-Wire bus. These commands also allow the master to determine how many and what types of devices are present on the bus or if any device has experienced an alarm condition. There are five ROM commands, and each command is 8 bits long. The master device must issue an appropriate ROM command before issuing a MY18E20 function command. A flowchart for operation of the ROM commands is shown in Figure 10.5-1.

SEARCH ROM [F0h]

When a system is initially powered up, the master must identify the ROM codes of all slave devices on the bus, which allows the master to determine the number of slaves and their device types. The master learns the ROM codes through a process of elimination that requires the master to perform a Search ROM cycle (i.e., Search ROM command followed by data exchange) as many times as necessary to identify all of the slave devices. If there is only one slave on the bus, the simpler Read ROM [33h] command can be used in place of the Search ROM process. After every Search ROM cycle, the bus master must return to Step 1 (Initialization) in the transaction sequence.

Read ROM [33h]

This command can only be used when there is one slave on the bus. It allows the bus master to read the slave’ s 64-bit ROM code without using the Search ROM procedure. If this command is used when there is more than one slave present on the bus, a data collision will occur when all the slaves attempt to respond at the same time.

Match ROM [55h]

The match ROM command followed by a 64-bit ROM code sequence allows the bus master to address a specific slave device on a multi-drop or single-drop bus. Only the slave that exactly matches the 64-bit ROM code sequence will respond to the function command issued by the master; all other slaves on the bus will wait for a reset pulse.

Skip ROM [CCh]

The master can use this command to address all devices on the bus simultaneously without sending out any ROM code information. For example, the master can make all MY18E20s on the bus perform simultaneous temperature conversions by issuing a Skip ROM command followed by a Convert T [44h] command.

Note that the Read Scratchpad [BEh] command can follow the Skip ROM command only if there is a single slave device on the bus. In this case, time is saved by allowing the master to read from the slave without sending the device’ s 64-bit ROM code. A Skip ROM command followed by a Read

Scratchpad command will cause a data collision on the bus if there is more than one slave since multiple devices will attempt to transmit data simultaneously.

Alarm Search [ECh]

The operation of this command is identical to the operation of the Search ROM command except that only slaves with a set alarm flag will respond. This command allows the master device to determine if any MY18E20s experienced an alarm condition during the most recent temperature conversion. After every Alarm Search cycle (i.e., Alarm Search command followed by data exchange), the bus master must return to Step 1 (Initialization) in the transaction sequence.

10.5 Function Commands

After the bus master has used a ROM command to address the MY18E20 with which it wishes to communicate, the master can issue one of the MY18E20 function commands. These commands allow the master to write to and read from the MY18E20 ' s scratchpad memory, initiate temperature conversions and determine the power supply mode. The MY18E20 function commands, which are described below, are summarized in Table 10.5 and illustrated by the flowchart in Figure 10.5-2.

CONVERT T [44h]

This command initiates a single temperature conversion. Following the conversion, the resulting thermal data is stored in the 2-byte temperature register in the scratchpad memory and the MY18E20 returns to its low-power idle state. The master can issue read time slots after the Conversion T command and the MY18E20 will respond by transmitting a 0 while the temperature conversion is in progress and a 1 when the conversion is done.

WRITE SCRATCHPAD [4Eh]

This command allows the master to write 3 bytes of data to the MY18E20' s scratchpad. The first data byte is written into the TH register (byte 2 of the scratchpad), the second byte is written into the TL register (byte 3), and the third byte is written into the configuration register (byte 4). Data must be transmitted least significant bit first. All three bytes MUST be written before the master issues a reset, or the data may be corrupted.

WRITE USER [66h]

This command allows the master to write 3 bytes of data to the MY18E20' s scratchpad. The first data byte is written into the User Byte 3 (byte 5 of the scratchpad), the second byte is written into the User Byte 4 (byte 6), and the third byte is written into the User Byte 5 (byte 7). Data must be transmitted least significant bit first. All three bytes MUST be written before the master issues a reset, or the data may be corrupted.

READ SCRATCHPAD [BEh]

This command allows the master to read the contents of the scratchpad. The data transfer starts with the least significant bit of byte 0 and continues through the scratchpad until the 9th byte (byte 8–CRC) is read. The master may issue a reset to terminate reading at any time if only part of the scratchpad data is needed.

COPY SCRATCHPAD [48h]

This command copies the contents of the scratchpad TH, TL and configuration registers (bytes 3, 4 and 5) to EEPROM.

RECALL E2 [B8h]

This command recalls the alarm trigger values (TH and TL) and configuration data from EEPROM and places the data in bytes 2, 3, and 4, respectively, in the scratchpad memory. The master device can issue read time slots following the Recall E2 command and the MY18E20 will indicate the status of the recall by transmitting 0 while the recall is in progress and 1 when the recall is done. The recall operation happens automatically at power-up, so valid data is available in the scratchpad as soon as power is applied to the device.

READ POWER SUPPLY [B4h]

The master device issues this command followed by a read time slot to determine the power mode of every MY18E20 on the bus. During the read time slot, externally powered MY18E20 will let the bus remain high. See the Power section for usage information for this command.

Table10.5 Function Command Set

COMMAND	DESCRIPTION	PROTOCOL	1-Wire BUS ACTIVITY AFTER COMMAND IS ISSUED	NOTES
TEMPERATURE CONVERSION COMMANDS				
Convert T	Initiates temperature conversion.	44h	MY18E20 transmits conversion status to master: When receives the read time slot, MY18E20 transmits a 0 while the conversion is in progress; MY18E20 transmits a 1 when the conversion is done.	
MEMORY COMMANDS				
Read Scratchpad	Reads the entire scratchpad including the CRC byte.	BEh	MY18E20 transmits up to 9 data bytes to master.	1
Write Scratchpad	Writes data into scratchpad bytes 2, 3, and 4 (T_H, T_L, and configuration registers).	4Eh	Master transmits 3 data bytes to MY18E20.	2

Write User	Writes data into scratchpad bytes 5, 6, and 7 (User Byte 3, 4, and 5).	66h	Master transmits 3 data bytes to MY18E20.	2
Copy Scratchpad	Copies T_H, T_L, configuration register, User Byte 3, User Byte 4 and User Byte 5 data from the scratchpad to EEPROM.	48h	None	
Recall E^2	Recalls T_H, T_L, and configuration register data from EEPROM to the scratchpad.	B8h	MY18E20 transmits recall status to master.	
Read Power Supply	Signals MY18E20 power supply mode to the master.	B4h	MY18E20 transmits supply status to master.	

Note :1 The master can interrupt the transmission of data at any time by issuing a reset.

2 All three bytes must be written before a reset is issued.

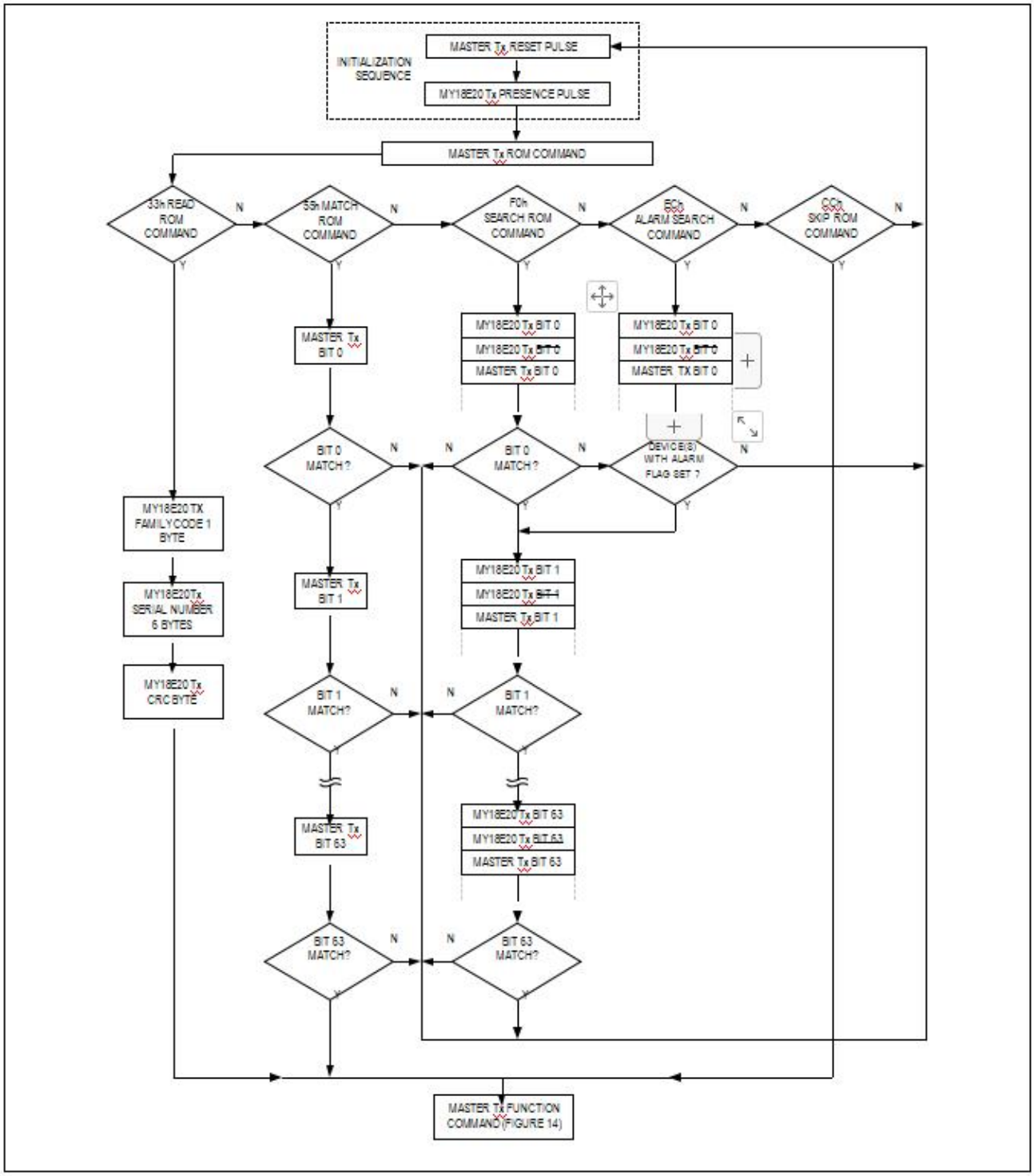


Figure10.5-1 ROM Commands Flowchart

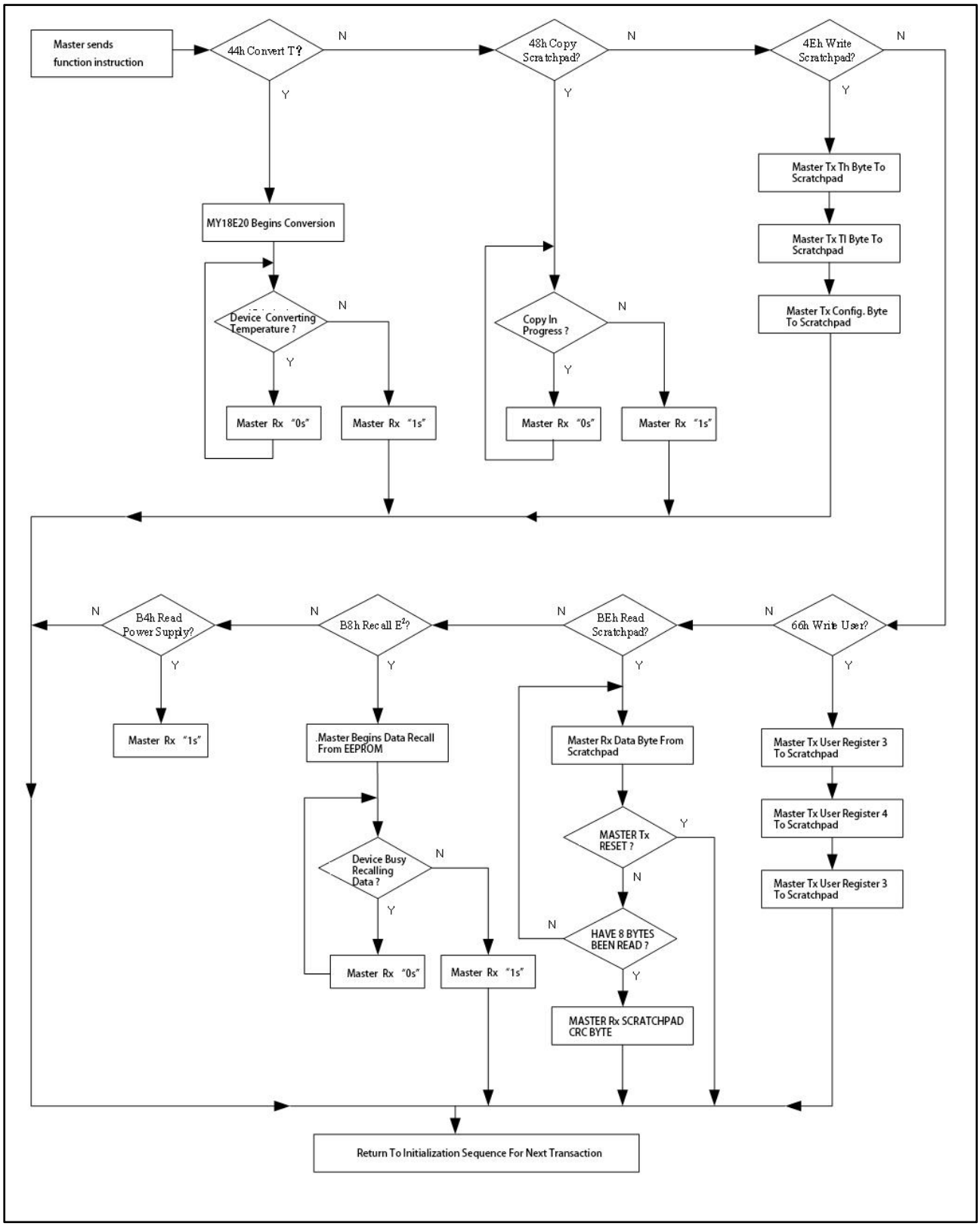


Figure 10. 5-2 Function Commands Flowchart

10.6 1-Wire Signaling

The MY18E20 uses a strict 1-Wire communication protocol to ensure data integrity. Several signal types are defined by this protocol: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. The bus master initiates all these signals, with the exception of the presence pulse.

Initialization Procedure — Reset And Presence Pulses

All communication with the MY18E20 begins with an initialization sequence that consists of a reset pulse from the master followed by a presence pulse from the MY18E20. This is illustrated in Figure 10.6-1. When the MY18E20 sends the presence pulse in response to the reset, it is indicating to the master that it is on the bus and ready to operate.

During the initialization sequence the bus master transmits (TX) the reset pulse by pulling the 1-Wire bus low for a minimum of 480µs. The bus master then releases the bus and goes into receive mode (RX). When the bus is released, the 5kΩ pullup resistor pulls the 1-Wire bus high. When the MY18E20 detects this rising edge, it waits 15µs to 60µs and then transmits a presence pulse by pulling the 1-Wire bus low for 60µs to 240µs.

Read/Write Time Slots

The bus master writes data to the MY18E20 during write time slots and reads data from the MY18E20 during read time slots. One bit of data is transmitted over the 1-Wire bus per time slot.

Write Time Slots

There are two types of write time slots: "Write 1" time slots and "Write 0" time slots. The bus master uses a Write 1 time slot to write a logic 1 to the MY18E20 and a Write 0 time slot to write a logic 0 to the MY18E20. All write time slots must be a minimum of 60µs in duration with a minimum of a 1µs recovery time between individual write slots. Both types of write time slots are initiated by the master pulling the 1-Wire bus low (see Figure 10.6-2).

To generate a Write 1 time slot, after pulling the 1-Wire bus low, the bus master must release the 1-Wire bus within 15µs. When the bus is released, the 5kΩ pullup resistor will pull the bus high. To generate a Write 0 time slot, after pulling the 1-Wire bus low, the bus master must continue to hold the bus low for the duration of the time slot (at least 60µs).

The MY18E20 samples the 1-Wire bus during a window that lasts from 15µs to 60µs after the master initiates the write time slot. If the bus is high during the sampling window, a 1 is written to the MY18E20. If the line is low, a 0 is written to the MY18E20.

Read Time Slots

The MY18E20 can only transmit data to the master when the master issues read time slots. Therefore, the master must generate read time slots immediately after issuing a Read Scratchpad [BEh] or Read Power Supply [B4h] command, so that the MY18E20 can provide the requested data. In addition, the master can generate read time slots after issuing Convert T [44h] or Recall E2 [B8h] commands to find out the status of the operation as explained in the MY18E20 Function Commands section.

All read time slots must be a minimum of 60µs in duration with a minimum of a 1µs recovery time between slots. A read time slot is initiated by the master device pulling the 1-Wire bus low for a minimum of 1µs and then releasing the bus (see Figure 10.6-2). After the master initiates the read time slot, the MY18E20 will begin transmitting a 1 or 0 on bus. The MY18E20 transmits a 1 by leaving the bus high and transmits a 0 by pulling the bus low. When transmitting a 0, the MY18E20 will release the bus by the end of the time slot, and the bus will be pulled back to its high idle state by the pullup resister. Output data from the MY18E20 is valid for 15µs after the falling edge that initiated the read time slot. Therefore, the master must release the bus and then sample the bus state within 15µs from the start of the slot.

Figure 10.6-3 illustrates that the sum of t_{INIT}, t_{RC}, and t_{SAMPLE} must be less than 15µs for a read time slot.
Figure 10.6-4 shows that system timing margin is maximized by keeping t_{INIT} and t_{RC} as short as possible and by locating the master sample time during read time slots towards the end of the 15µs period.

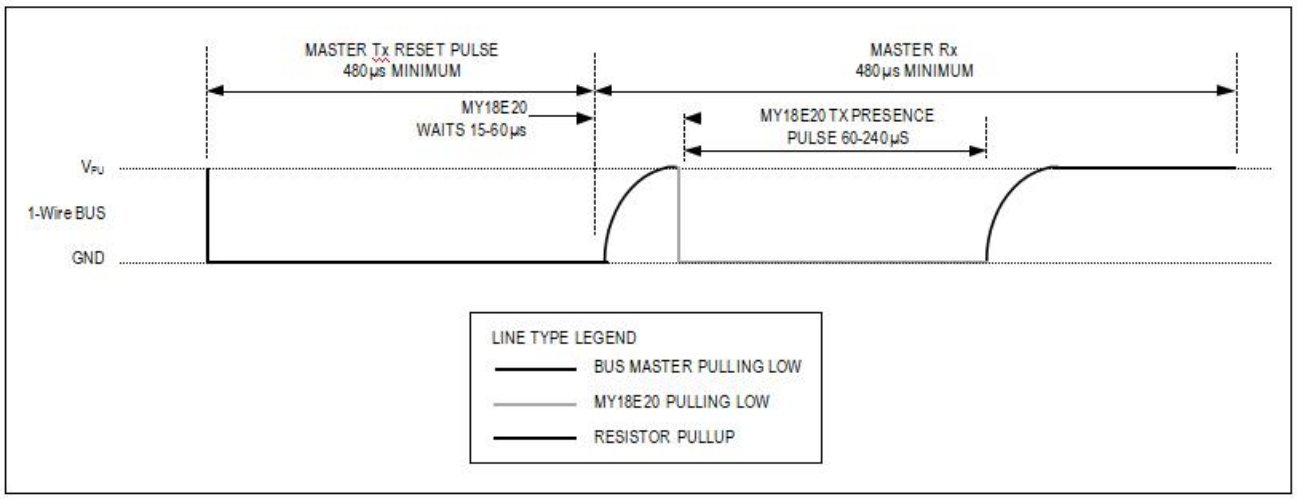


Figure10.6-1 Initialization Timing

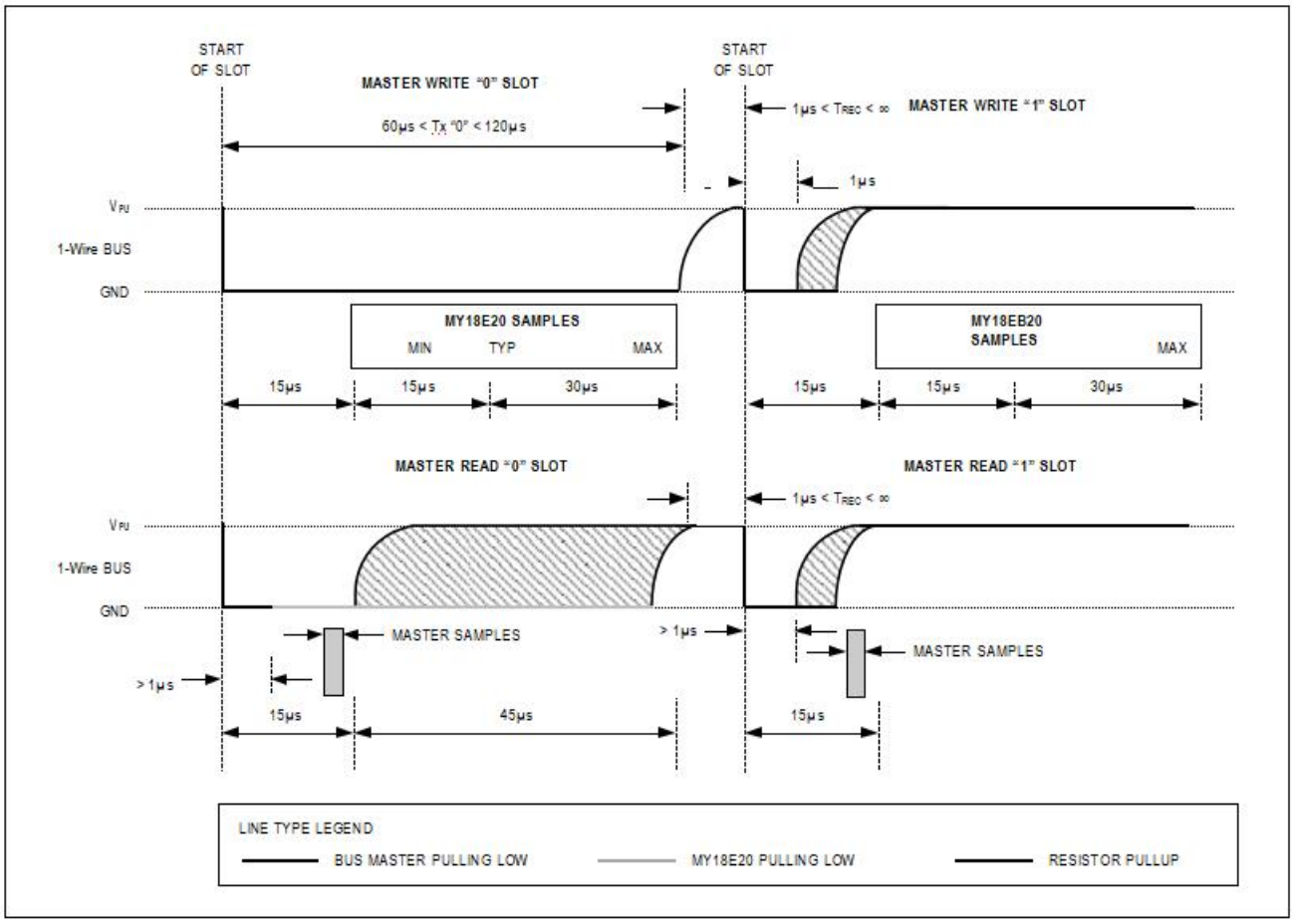


Figure10.6-2 Read/Write Time Slot Timing Diagram

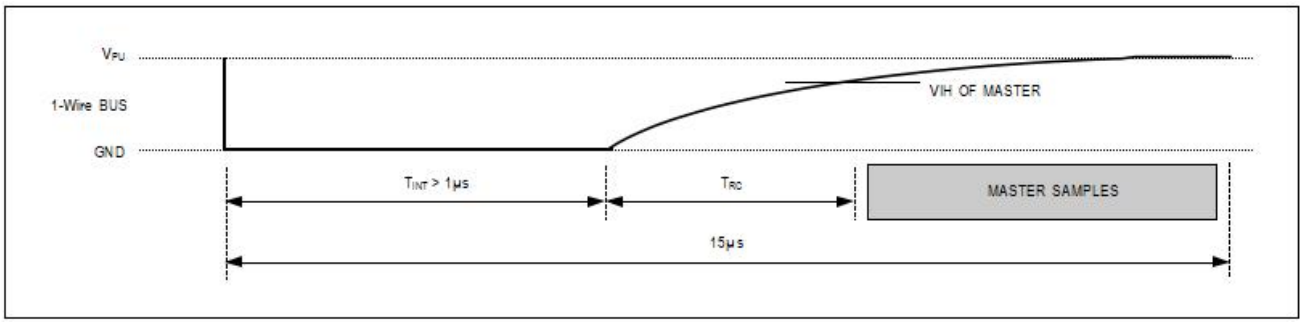


Figure10.6-3 Detailed Master Read 1 Timing

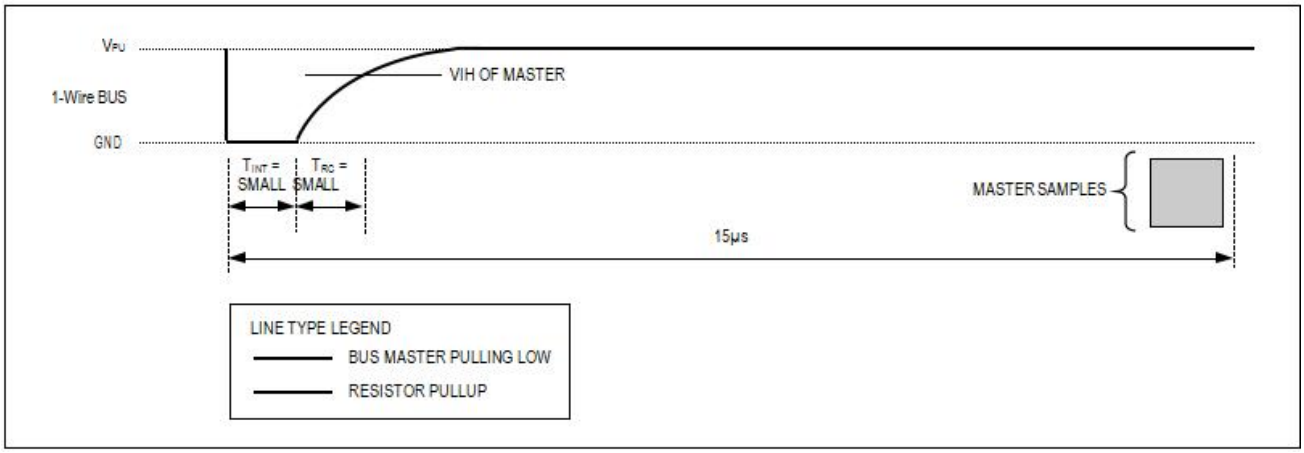


Figure10.6-4 Recommended Master Read 1 Timing

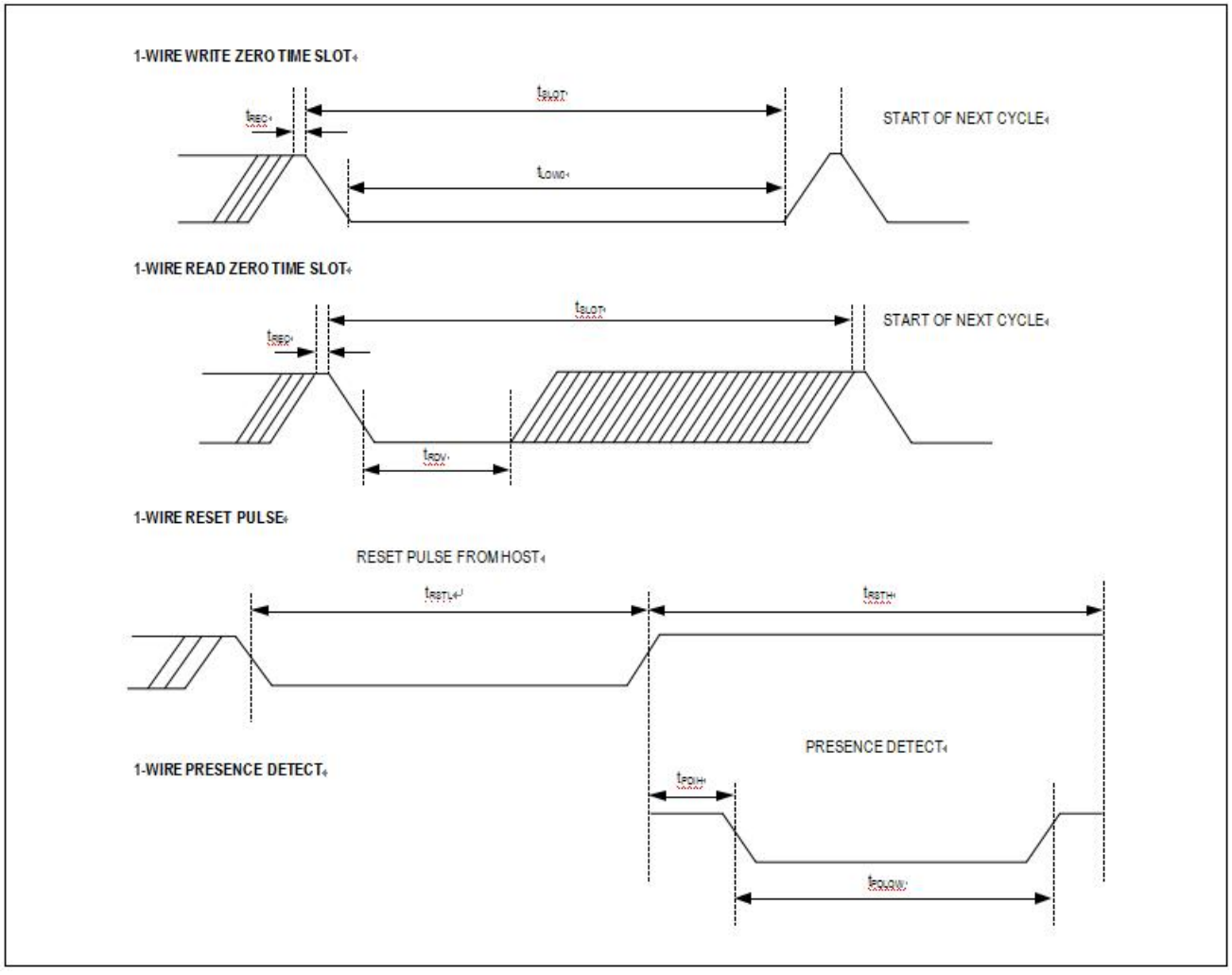


Figure10.6-5 Timing Diagrams

10.7 Operation Example 1

In this example there are multiple MY18E20s on the bus. The bus master initiates a temperature conversion in a specific MY18E20 and then reads its scratchpad and recalculates the CRC to verify the data.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
Tx	Reset	Master issues reset pulse.
Rx	Presence	MY18E20s respond with presence pulse.
Tx	55h	Master issues Match ROM command.
Tx	64-bit ROM code	Master sends MY18E20 ROM code.
Tx	44h	Master issues Convert T command.
Tx	DQ line held high by strong pullup	Master applies strong pullup to DQ for the duration of the conversion (t_{CONV}).
Tx	Reset	Master issues reset pulse.
Rx	Presence	MY18E20s respond with presence pulse.
Tx	55h	Master issues Match ROM command.
Tx	64-bit ROM code	Master sends MY18E20 ROM code.
Tx	BEh	Master issues Read Scratchpad command.
Rx	9 data bytes	Master reads entire scratchpad including CRC. The master then recalculates the CRC of the first eight data bytes from the scratchpad and compares the calculated CRC with the read CRC (byte 9). If they match, the master continues; if not, the read operation is repeated.

10.8 Operation Example 2

In this example there is only one MY18E20 on the bus. The master writes to the TH, TL, and configuration registers in the MY18E20 scratchpad and then reads the scratchpad and recalculates the CRC to verify the data. The master then copies the scratchpad contents to EEPROM.

MASTER MODE	DATA (LSB FIRST)	COMMENTS
Tx	Reset	Master issues reset pulse.
Rx	Presence	MY18E20 responds with presence pulse.
Tx	CCh	Master issues Skip ROM command.
Tx	4Eh	Master issues Write Scratchpad command.
Tx	3 data bytes	Master sends three data bytes to scratchpad (TH, TL, and config).
Tx	Reset	Master issues reset pulse.
Rx	Presence	MY18E20 responds with presence pulse.
Tx	CCh	Master issues Skip ROM command.

Tx	BEh	Master issues Read Scratchpad command.
Rx	9 data bytes	Master reads entire scratchpad including CRC. The master then recalculates the CRC of the first eight data bytes from the scratchpad and compares the calculated CRC with the read CRC (byte 9). If they match, the master continues; if not, the read operation is repeated.
Tx	Reset	Master issues reset pulse.
Rx	Presence	MY18E20 responds with presence pulse.
Tx	CCh	Master issues Skip ROM command.
Tx	48h	Master issues Copy Scratchpad command.
Tx	DQ line held high by strong pullup	Master applies strong pullup to DQ for at least 10ms while copy operation is in progress.

11. Electrical Characteristics

11.1 Absolute maximum rating

Voltage Range on Any Pin Relative to Ground.....-0.5V to +6.0V
Operating Temperature Range..... -55°C to +125°C
Storage Temperature Range..... -55°C to +125°C
Solder Temperature..... Refer to the IPC/JEDEC J-STD-020 Specification

Note:These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

11.2 DC Electrical Characteristics

-55℃ to +125℃; VDD=1.8V to 5.5V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTE
Supply Voltage	V_{DD}		+1.8	—	+5.5	V	1
Thermometer Error	t_{ERR}	-10°Cto+85°C	—	—	±0.5	°C	
		-55°Cto+125°C	—	—	±1.5		
Input Logic-Low	V_{IL}	5V	—	1.46	—	V	1,2
		3V	—	0.95	—		
Input Logic-High	V_{IH}	5V	—	1.56	—	V	1,3
		3V	—	1.08	—		
Sink Current	I_L	$V_{I/O}$=0.4V	4.0	—	—	mA	1
Standby Current	I_{DDS}	—	—	0.2	1	μA	4
Active Current	I_{DD}	V_{DD}=5V	—	40	350	μA	5
Waiting time before	t_{PU}	—	—	2	—	ms	

entering idle state after power up							
DQ Input Current	I_{DQ}	—	—	5	—	μA	6
Pull Up Resistor	R_{UP}	—	1	2.2	4.7	KΩ	7
Pullup Supply Voltage	V_{UP}	—	+1.8	—	+5	V	1,8

Note :1 All voltages are referenced to ground.

2 Logic-low voltages are specified at a sink current of 1mA.

3 Standby current specified up to +70°C. Standby current typically is 3μA at +125°C.

4 To minimize IDDS, DQ should be within the following ranges: GND ≤ DQ ≤ GND + 0.3V or VDD − 0.3V ≤ DQ ≤ VDD

5 Active current refers to supply current during active temperature conversions or EEPROM writes.

6 DQ line is high ("high-Z" state).

7 R_{UP} refers to the resistance value between DQ and VDD.

8 In order not to affect long cable communication, the range of 3.3V~5V is recommended.

11.3 AC Electrical Characteristics–NV Memory

-55℃ to +125℃; V_{DD}=1.8V to 5.5V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
NV Write Cycle Time	t_{WR}	—		—	40	ms
EEPROM Writes	N_{EEWR}	-55°C to +55°C	50k			writes
EEPROM Data Retention	t_{EEDR}	-55°C to +55°C	10			years

11.4 AC Electrical Characteristics

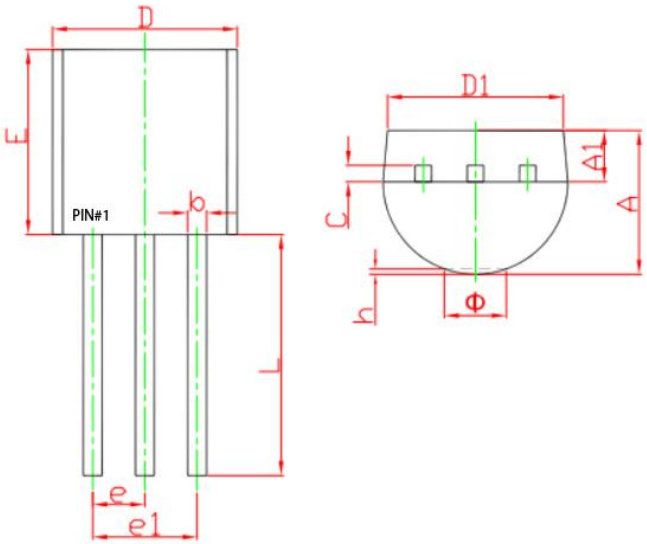
-55℃ to +125℃; V_{DD}=1.8V to 5.5V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Temperature Conversion Time	t_{CONV}	Note	15	100	500	ms
Time Slot	t_{SLOT}	Note	60	—	120	μs
Recovery Time	t_{REC}	Note	1	5	—	μs
Write 0 Low Time	t_{LOW0}	Note	60	60	120	μs
Write 1 Low Time	t_{LOW1}	Note	1	5	15	μs
Read Data Valid	t_{RDV}	Note	—	5	15	μs
Reset Time Low	t_{RSTL}	Note	480	960	—	μs
Presence-Detect High	t_{PDHIGH}	Note	15	30	60	μs
Presence-Detect Low	t_{PDLOW}	Note	60	115	240	μs

Note: See the timing diagrams in Figure 10.6.5.

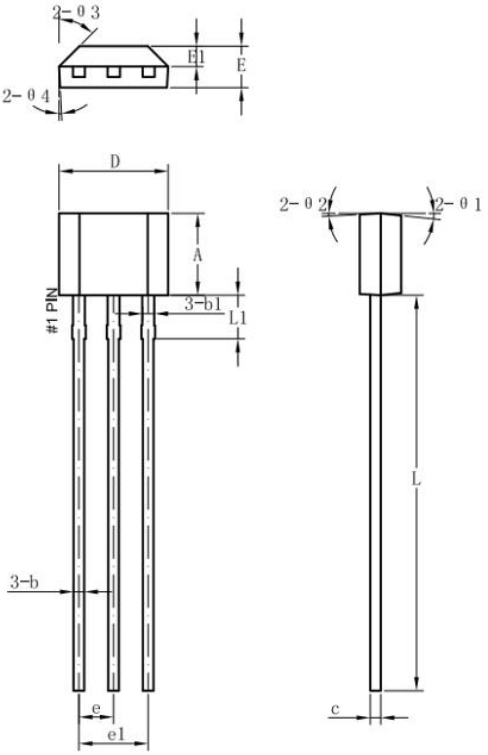
12 Package

12.1MY18E20/MY18E20-15（TO-92）



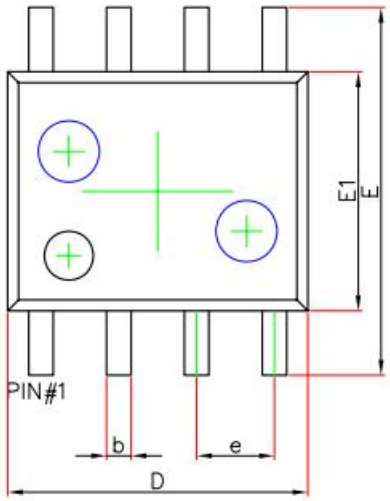
SYMBOL	MILLIMETER			INCH		
	MIN	TYP	MAX	MIN	TYP	MAX
A	3.300	3.500	3.700	0.130	0.138	0.146
A1	1.100	1.250	1.400	0.043	0.049	0.055
b	0.380	0.465	0.550	0.015	0.018	0.022
c	0.360	0.435	0.510	0.014	0.017	0.020
D	4.300	4.500	4.700	0.169	0.177	0.185
D1	3.430	—	—	0.135	—	—
E	4.300	4.500	4.700	0.169	0.177	0.185
e	1.270TYP.			0.050TYP.		
e1	2.440	2.540	2.640	0.096	0.100	0.104
L	14.100	14.300	14.500	0.555	0.563	0.571
Φ	—	—	1.600	—	—	0.063
h	0	0.190	0.380	0.000	0.007	0.015

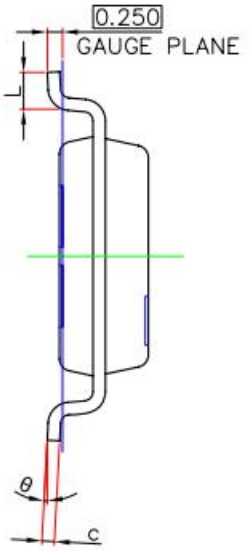
12.2 MY1820/MY1820-15（TO-92S）

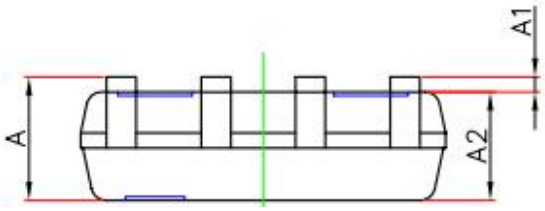


SYMBOL	MILLIMETER			INCH		
	MIN	TYP	MAX	MIN	TYP	MAX
A	2.900	3.000	3.100	0.114	0.118	0.122
b	0.350	0.390	0.560	0.014	0.015	0.022
b1		0.440			0.017	
c	0.360	0.380	0.510	0.014	0.015	0.020
D	3.900	4.000	4.100	0.154	0.157	0.161
E	1.420	1.520	1.620	0.056	0.060	0.064
E1		0.750			0.030	
e		1.270			0.050	
e1		2.540			0.100	
L	13.500	14.500	15.500	0.531	0.571	0.610
L1		1.600			0.063	

12.3 MY18B20Z/MY18B20Z-15（SOP8）

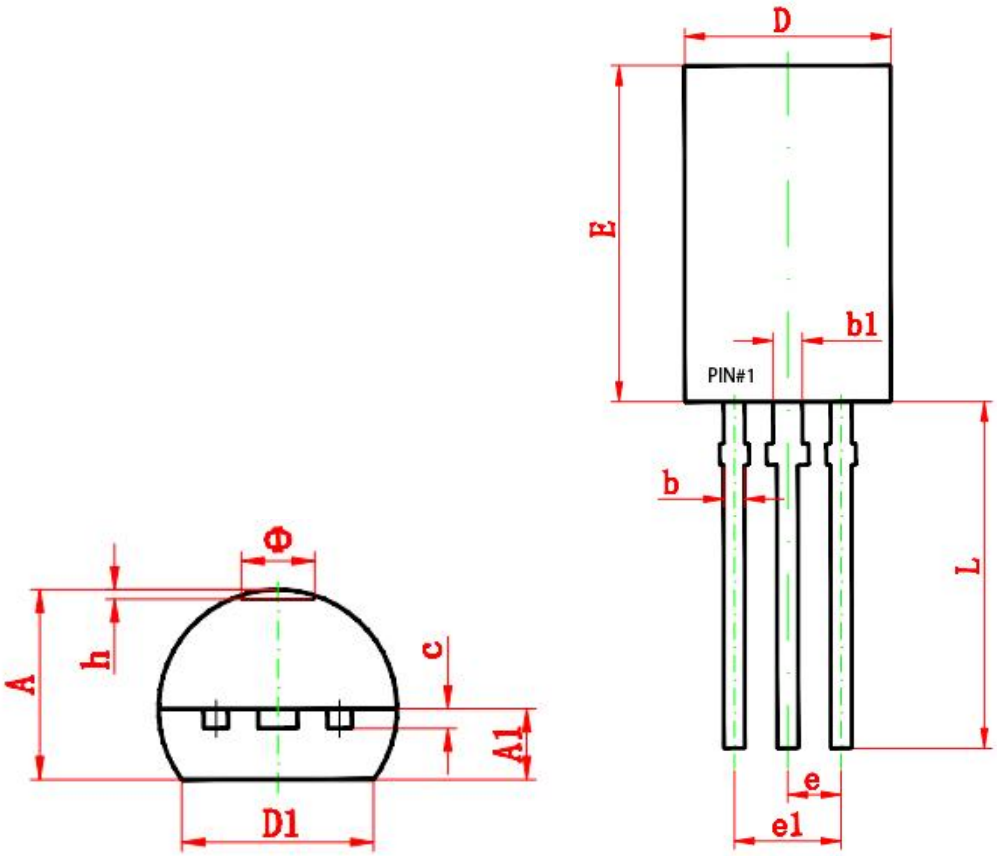






SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.450	1.750	0.057	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

12.4 MY18B20L/MY18B20L-15（TO-92L）



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	3.750	4.050	0.148	0.159
A1	1.280	1.580	0.050	0.062
b	0.380	0.550	0.015	0.022
b1	0.620	0.780	0.024	0.031
c	0.350	0.450	0.014	0.018
D	4.750	5.050	0.187	0.199
D1	3.900	4.100	0.154	0.161
E	7.850	8.150	0.309	0.321
e	1.270 TYP.		0.050 TYP.	
e1	2.440	2.640	0.096	0.104
L	13.800	14.200	0.543	0.559
Φ		1.600		0.063
h	0.000	0.300	0.000	0.012